AMENDMENTS TO THE CLAIMS

1. (Original) A content addressable memory (CAM) system comprising:

a ternary CAM array segmented into a plurality of array groups, each array group including a plurality of rows of ternary CAM cells; and

a plurality of first storage elements each for storing a priority of a corresponding array group.

2. (Original) The CAM system of Claim 1, wherein two or more array groups have the same priority.

3. (Original) The CAM system of Claim 1, wherein one of the rows of ternary CAM cells comprises:

a plurality of CAM cells for storing a data word; and

a plurality of mask cells for storing a local mask word.

4. (Original) The CAM system of Claim 3, wherein each data word comprises a policy statement.

5. (Original) The CAM system of Claim 4, wherein the policy statement comprises protocol information.

6. (Original) The CAM system of Claim 4, wherein the policy statement comprises type-of-service information.

7. (Original) The CAM system of Claim 4, wherein the policy statement comprises cost-of-service information.

8. (Original) The CAM system of Claim 4, wherein each local mask word includes a policy mask.

9. (Original) The CAM system of Claim 1, further comprising a plurality of second storage elements each for storing a group valid bit indicating whether an associated array group is assigned its corresponding priority number.

10. (Original) The CAM system of Claim 1, further comprising a priority table including the plurality of first storage elements.

11. (Original) The CAM system of Claim 1, further comprising an index circuit coupled to the ternary CAM array to determine the index of a location in the ternary CAM array that stores data that matches a search key.

12. (Original) The CAM system of Claim 11, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive match signals from the plurality of array groups, each match signal indicative of a result of a comparison between the search key and the data stored in the array groups, and having a plurality of outputs to provide qualified match signals for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified match signals, and having an output to provide the index of the highest priority location in the ternary CAM array that stores data that matches the search key in response to the qualified match signals.

13. (Original) The CAM system of Claim 12, wherein the select circuit includes means for selectively forcing non-qualified match signals to a mismatch state.

14. (Original) The CAM system of Claim 12, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the match signals from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the match signals to the priority encoder as qualified match signals in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priorities associated with array groups that have data stored that matches the search key.

15. (Original) The CAM system of Claim 14, further comprising a priority table including the plurality of first storage elements.

16. (Original) The CAM system of Claim 15, wherein the select circuit further comprises a plurality of group match flag circuits, each receiving the match signals from a corresponding array group and generating a group match flag in response thereto, wherein the group match flags are provided as select signals to corresponding rows of the priority table.

17. (Original) The CAM system of Claim 1, further comprising:
means for storing data in the array groups according to priority.

18. (Original) The CAM system of Claim 1, further comprising an address circuit coupled to the ternary CAM array to select a row of the ternary CAM cells for communicating data.

19. (Original) The CAM system of Claim 18, wherein the address circuit comprises an address decoder to select a row in one array group corresponding to the priority in response to a next free address (NFA).

20. (Original) The CAM system of Claim 19, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a corresponding priority.

21. (Original) The CAM system of Claim 20, wherein each row in the NFA table includes an empty bit storage element for storing an empty bit indicative of whether any array group is assigned to the corresponding priority.

22. (Original) The CAM system of Claim 9, wherein each of the rows of ternary CAM cells includes a valid bit storage element for storing a valid bit indicative of whether the corresponding row of ternary CAM cells stores valid data.

23. (Original) The CAM system of Claim 9, further comprising an index circuit coupled to the valid bit storage elements to determine a next free array address for an array group and its associated priority, and further coupled to the plurality of second storage elements to determine a next free group address for the array group and its associated priority.

24. (Original) The CAM system of Claim 23, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive the valid bits from the plurality of array groups, and having a plurality of outputs to provide qualified valid bits for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified valid bits, and having an output to generate the next free array address in response to the qualified valid bits.

25. (Original) The CAM system of Claim 24, wherein the select circuit includes means for selectively forcing non-qualified valid bits to a mismatch state.

26. (Original) The CAM system of Claim 24, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the array groups.

27. (Original) The CAM system of Claim 24, wherein the index circuit further comprises:

a group priority encoder having a plurality of inputs to receive the group valid bits from each of the plurality of array groups, and having an output to provide the next free group address.

28. (Twice Amended) A method of operating a content addressable memory (CAM) system including an array of ternary CAM cells segmented into a plurality of array groups, comprising:

storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups, wherein each array group includes a plurality of rows of the ternary CAM cells; and

selectively storing data in the array groups according to the priorities.

29. (Original) The method of Claim 28, wherein the selectively storing data comprises:

providing a next free address (NFA) of an available row of ternary CAM cells within an array group corresponding to one of the priorities; and

storing the data at the NFA.

30. (Previously Amended) A method of operating a content addressable memory (CAM) system including an array of ternary CAM cells segmented into a plurality of array groups, comprising:

storing a plurality of priorities in a plurality of storage elements each associated with one or more of the array groups; and

selectively storing data in the array groups according to the priorities,

wherein the selectively storing data comprises:

providing a next free address (NFA) of an available row of ternary CAM cells within an array group corresponding to one of the priorities; and

storing the data at the NFA; and

wherein providing the NFA comprises:

generating the NFA;

storing the NFA in a corresponding row of an NFA table;

selecting a row of the NFA table using the priority; and

accessing the NFA corresponding to the priority.

31. (Original) The method of Claim 30, wherein generating the NFA comprises:

for each array group, comparing associated priorities of the data with the priority of the array group to generate an enable signal;

selectively allowing, in response to the enable signals, valid bits from corresponding array groups to participate in the generation of the NFA, the valid bits indicating whether valid data is stored in corresponding rows of each array group.

32. (Original) The method of Claim 31, wherein the selectively allowing comprises:

selectively qualifying the valid bits from each array group in response to the corresponding enable signal to generate qualified valid bits; and

generating the NFA in response to the qualified valid bits.

33. (Original) The method of Claim 31, wherein the generating the NFA further comprises:

for each array group, storing a group valid bit indicative of whether the array group is assigned to one of the priorities; and

generating a first portion of the NFA in response to the group valid bits.

34. (Original) The method of Claim 28, further comprising:

selectively comparing a search key with data stored in the array groups.

35. (Original) The method of Claim 34, wherein the selectively comparing comprises:

comparing the search key with data stored in the array groups to generate match signals;

comparing the associated priorities of each array group that includes data that matches the search key to generate a plurality of enable signals; and

selectively qualifying the match signals in response to the enable signals to generate qualified match signals.

36. (Original) The method of Claim 35, further comprising:

generating an index of the highest priority match (HPM) in response to the qualified match signals.